What is Claimed is:

1. A package including:

a circuit board;

an set of circuit elements on the circuit board, the set of circuit elements including at least one integrated circuit and passive components; and

packaging material surrounding the set of circuit elements and part of the circuit board, wherein one side of the circuit board includes a set of terminals that are visible from the side of the package, the set of terminals being positioned away from the edge of the circuit board.

2. The package of claim 1, wherein the packaging material includes molded plastic.

3. The package of claim 2, wherein the packaging material includes a bordering frame.

4. The package of claim 1, wherein one side of the circuit board is exposed.

5. The package of claim 4, wherein the exposed side of the circuit board material includes the set of terminals connected to the remainder of the circuit board by vias.

6. The package of claim 5, wherein the circuit board material is attached to the packaging material by epoxy.

7. The package of claim 1, wherein the circuit elements includes at least two integrated circuits and passive devices.

8. The package of claim 7, wherein the thickness of the package is less than 12 mils.

9. The package of claim 1, wherein the package is a flash EEPROM package.

10. A package including:

a circuit board;

at least one integrated circuit on the circuit board; and

packaging material surrounding the set of circuit elements and part of the circuit board, wherein one side of the circuit board is exposed, the exposed side of the circuit board material including a set of terminals connected to the remainder of the circuit board by vias.

11. The package of claim 10, wherein the circuit board material is attached to the packaging material by epoxy.

12. The package of claim 10, wherein on the exposed side of the circuit board only the set of terminals is exposed.

13. The package of claim 10, wherein the circuit elements includes at least two integrated circuits and passive devices.

14. The package of claim 10, wherein the thickness of the package is less than 12 mils.

15. The package of claim 10, wherein the package is a flash EEPROM package.

16. A package including:

a circuit board;

an set of circuit elements on the circuit board, the set of circuit elements including at least one integrated circuit and passive components; and

a plastic material encasing the set of circuit elements and part of the circuit board, wherein one side of the circuit board includes a set of terminals that are accessible from the side of the package, the set of terminals being positioned away from the edge of the circuit board.

17. The package of claim 16, wherein one side of the circuit board is exposed.

18. The package of claim 17, wherein the exposed side of the circuit board material includes the set of terminals connected to the remainder of the circuit board by vias.

19. The package of claim 16, wherein the circuit board material is attached to the packaging material by epoxy.

20. The package of claim 16, wherein on the exposed side of the circuit board only the set of terminals is exposed.

21. The package of claim 16, wherein the thickness of the package is less than 12 mils.

22. The package of claim 16, wherein the package is a flash EEPROM package.

23. A method comprising:

attaching an set of circuit elements to a circuit board, the set of circuit elements including at least one integrated circuit and passive components; and

thereafter, packaging the circuit board in plastic such that one side of the circuit board includes a set of terminals that are accessible from the side of the package.

24. The method of claim 23, wherein the packaging step includes placing plastic into a mold containing the circuit board.

25. The method of claim 24, wherein the packaging step includes clamping over terminals.

26. The method of claim 23, wherein the packaging step includes putting plastic into a mold with multiple chambers, each chamber having a different circuit board.

27. The method of claim 23, wherein the packaging step includes putting the circuit board in a border frame.

28. The method of claim 23, wherein the circuit board elements include two integrated circuits and the method further comprises
a first encapsulating step for the two integrated circuits.

29. The method of claim 23, wherein the first encapsulating step is such that there is a connecting region of encapsulant material formed between the two integrated circuits, the connecting region of encapsulant material being narrower than the integrated circuits.

30. A method comprising:

providing a circuit board with at least two integrated circuits formed thereon; and

encapsulating the at least two integrated circuits in an encapsulant material, the encapsulating step being such that there is a connecting region of encapsulant material formed between two of the at least two integrated circuits, the connecting region of encapsulant material being narrower than the two of the at least two integrated circuits.

31. The method of claim 31, further comprising, after the encapsulating step, packaging the circuit board.

32. A method comprising:

attaching an set of circuit elements to a circuit board, the set of circuit elements including at least one integrated circuit and passive components, the circuit board having test connections and terminals, the test connections being connected to test the set of circuit elements;

testing the set of circuit elements using the test connections;

thereafter, removing the test connections portion of the circuit board; and

thereafter, packaging the circuit board.

33. The method of claim 32, wherein the terminals are positioned on a side of the circuit board.

34. The method of claim 32, wherein the package is such that the terminals are exposed.

35. The method of claim 32, wherein the testing includes a burn-in testing.

36. The method of claim 32, further comprising programming at least one integrated circuit using the test connections.